Kindly **add** the following claims:

151. A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:

a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request.

152. The synchronous memory device of claim 151 wherein the value which is representative of the delay time is stored in the register after power is applied to the device.

153. The synchronous memory device of claim 151 wherein the value which is representative of the delay time is stored in the register after the memory device is reset.

154. The synchronous memory device of claim 151 wherein the value which is representative of a delay time is stored in the register when the memory device is initialized.

155. The synchronous semiconductor memory device of claim 151 wherein, in response to a set register request, the value which is representative of a delay time is stored in the programmable register.

156. The synchronous semiconductor memory device of claim 155 wherein the control register access and the value which is

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representative of a delay time are provided to the memory device in a single request packet.

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157. A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprising:

a programmable register to store a value which is representative of a programmable delay time after which the memory device responds to a transaction request; and

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wherein the memory device responds to a first transaction request in accordance with a fixed delay time and, after programming the programmable register, responds to the second transaction request in accordance with the programmable delay time.

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158. The synchronous semiconductor memory device of claim 157 further including a pre-programmed register to store a value which is representative of the fixed delay time.

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159. The synchronous semiconductor memory device of claim 157 wherein the value which is representative of the programmable delay time is stored in the programmable register after power is applied to the synchronous memory device.

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160. The synchronous semiconductor memory device of claim 157 wherein the value which is representative of the programmable delay time is stored in the programmable register after the memory device is reset.

bb

161. The synchronous semiconductor memory device of claim 157 wherein the value which is representative of the programmable delay time is stored in the programmable register after the memory device is initialized.

162. The synchronous semiconductor memory device of claim 157 wherein, in response to a ~~set register request~~ control register access, the value which is representative of the programmable delay time is stored in the programmable register.

163. The synchronous semiconductor memory device of claim 162 wherein the ~~set register request~~ control register access and the value which is representative of the programmable delay time are provided to the memory device in a single request packet.

164. A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprising:

a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request; and

a plurality of drivers to output data in response to the read request, wherein the drivers output data on a bus in accordance with the delay time.

165. The synchronous memory device of claim 164 wherein the value which is representative of the delay time is stored in the register after power is applied to the device.

166. The synchronous memory device of claim 164 wherein the value which is representative of a delay time is stored in the register when the memory device is initialized.

167. The synchronous semiconductor memory device of claim 164 wherein, in response to a set register request, the value which is representative of a delay time is stored in the programmable register.

168. A method of controlling the operation of a synchronous semiconductor memory device wherein the memory device includes a register, the method comprising:

storing a time-delay value in the register in the memory device, the time-delay value being representative of a time delay after which the memory device responds to a transaction request.

169. The method of claim 168 further including issuing a ~~set register request~~ control register access wherein, in response to the ~~set register request~~ control register access, the memory device stores a time delay value in the register.

170. The method of claim 168 wherein the ~~set register request~~ control register access and the time delay value are provided to the memory device in a single request packet.

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21 ~~171~~. The method of claim ~~168~~ 18 further including initializing the register by providing a time delay value to the memory device after issuing a ~~set register request~~ control register access.

22 ~~172~~. The method of claim ~~171~~ 21 wherein the ~~set register request~~ control register access and the time delay value are provided to the memory device in a single request packet.

23 ~~173~~. The method of claim ~~168~~ 18 further including initializing the register after the memory device is powered-up or reset.

24 ~~174~~. The method of claim ~~168~~ 18 further including ~~the step of~~ selecting one of a plurality of time delays after which the memory device is to provide data in response to a read request.

25 ~~175~~. The method of claim ~~168~~ 18 wherein the transaction request is a read request.

26 ~~176~~. The method of claim ~~169~~ 19 wherein the transaction request is a write request.

REMARKS

This Preliminary Amendment seeks to place this application in condition for allowance. The instant application is a continuation of Application Serial No. 08/798,520. Application Serial No.

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